REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on April 21, 2006.

In this Amendment, claim 24 is canceled, claims 1, 23, 25, and 26 are amended, and claims 27-31 are added so that claims 1-9, 21-23, and 25-31 are pending and subject to examination.

I. 35 USC 102(e) - Tsuda et al.

In the Office Action, claims 1, 4-6, 23, 24, and 26 are rejected as being anticipated by Tsuda et al. (U.S. Patent Publication No. 2002/0047501). This rejection is traversed.

However, to expedite the prosecution of the application, independent claim 1 has been amended. Independent claim 1 now recites a method comprising, *inter alia*, "wherein after mounting, the leads have surfaces that are substantially coplanar with the exterior surface of the molding material and the surface of the die with the electrical terminal, and wherein the surface of the die with the electrical terminal is exposed by the window in the molding material." An example of this feature is shown in FIGS. 1(b) and 1(c). As shown in FIG. 1(b), the bottom surface or backside 30(a) of the die 30 forms an electrical terminal, and is substantially coplanar with an exterior surface of the molding material 11, and the leads of the leadframe structure in the package. As shown in FIG. 1(c), this allows the package 100 to be mounted on a circuit substrate 55 or the like. Clearly, Tsuda et al. fails to teach or suggest a package with "leads [that] have surfaces that are substantially coplanar with the exterior surface of the molding material and the surface of the die with the electrical terminal, and wherein the surface of the die with the electrical terminal is exposed by the window in the molding material." Dependent claims 2-6, 23, and 26 are allowable, since they depend from independent claim 1.

II. 35 USC 103 - Tsuda et al. and Kasem et al.

Claims 2, 3, 7-9, 22, and 25 are rejected as being obvious over Tsuda and Kasem et al. (U.S. Patent No. 6,392,290). The Examiner admits that Tsuda et al. does not teach a plurality of leads including a source lead and a gate lead, or a vertical power MOSFET, but alleges that Kasem et al. teaches these features and that one would have used them in Tsuda et al.'s device. The Examiner alleges the following:

> Kasem gives motivation in col. 1, lines 36-57. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Kasem's process with Tsuda's invention would be beneficial because it is a less expensive and simpler way to form a vertical power MOSFET.

This rejection is traversed.

1. Contrary to the obviousness rejection, one would not have been led to modify Tsuda et al. with the process in Kasem et al. for the alleged reasons at column 35-48 of Kasem et al.

One would not have been led to modify Tsuda et al. with the process in Kasem et al. for the reasons provided by the Examiner. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). MPEP 2143.01. Here, the Examiner alleges that one skilled in the art would have modified Tsuda et al.'s "Surface Acoustic Wave Device" (see Tsuda et al.'s title) with a leadframe structure with a source lead and a gate lead, and with a vertical power MOSFET for the reasons provided at column 1, lines 35-48 of Kasem et al. To put his passage into context, column 1, lines 15-57 of Kasem et al. are reproduced below:

> After the processing of a semiconductor wafer has been completed, the resulting semiconductor chips, which could be integrated circuit (IC) or MOSFET chips for example, must be separated and packaged in such a way that they can be connected to external circuitry. There are many known packaging techniques. Most

> involve mounting the chip on a leadframe, connecting the chip pads to the leadframe by wire-bonding or otherwise, and then encapsulating the chip and wire bonds in a plastic capsule, with the leadframe left protruding from the capsule. The encapsulation is often done by injection-molding. The leadframe is then trimmed to remove the tie bars that hold it together, and the leads are bent in such a way that the package can be mounted on a flat surface, typically a printed circuit board (PCB).
>
> This is generally an expensive, time-consuming process, since the individual chips are typically handled separately. Moreover, the resulting semiconductor package is considerably larger than the chip itself, using up an undue amount of scarce "real estate" on the PCB. In addition, wire bonds are fragile and introduce a considerable resistance between the chip pads and the leads of the package.
>
> The problems are particularly difficult when the device to be packaged is a "vertical" device, having terminals on opposite faces of the chip. For example, a power MOSFET typically has its source and gate terminals on the front side of the chip and its drain terminal on the back side of the chip. Similarly, a vertical diode has its anode terminal on one face of the chip and its cathode terminal on the opposite face of the chip. Bipolar transistors, junction field effect transistors (JFETs), and various types of integrated circuits (ICs) can also be fabricated in a "vertical" configuration, as can passive components such as semiconductor capacitors or resistors.
>
> Accordingly, there is a need for a process which is simpler and less expensive than existing processes and which produces a package that is essentially the same size as the chip. There is a particular need for such a process and package that can be used with semiconductor dice having terminals on both their front and back sides. For reasons of economy and enhanced performance, it is desirable that the process be performed on all of the chips in the wafer form before they are separated from each other, i.e., that the process be vertical wafer-level chip-scale packaging.

This passage from Kasem et al. discusses the problems associated with packaging vertical power MOSFET devices. As explained above, a conventionally packaged vertical MOSFET takes up scarce real estate on a circuit board, because source and gate terminals are at a front side of a

chip and a drain terminal is at a back side of the chip. Kasem et al. attempts to solve this problem by routing a drain connection to the same side of the chip as the source connection and gate connection. This is done by providing a via through the chip (see "Si Via" in FIG. 3A of Kasem et al.). According to Kasem et al., this allows one to make a package that is compact and that can be mounted using a flip chip process (see Kasem et al.'s abstract).

Contrary to the Office Action, the alleged motivation at col. 1, lines 35-47 of Kasem et al. does not provide a reason why it would be advantageous for one to have used a power MOSFET and a leadframe structure with a source lead and a gate lead. Rather, col. 1, lines 35-47 of Kasem et al. provides background as to why one would want to route a drain connection to the same side of the chip as a source connection and a gate connection. Put another way, col. 1, lines 35-47 of Kasem et al. does not suggest that one skilled in the art should use a power MOSFET or a leadframe structure with a source lead and a gate lead, but suggests that one might want to use Kasem et al.'s drain connection routing method, because the resulting power MOSFET takes up less real estate than a conventional power MOSFET. Since Tsuda et al.'s device is a surface acoustic wave device and is not a power MOSFET, Kasem et al.'s drain connection method would have no benefit for Tsuda et al.'s surface acoustic wave device.

Moreover, one would not have been led to modify Tsuda et al. for the reason proposed by the Examiner, since modifying Tsuda et al. to include a vertical power MOSFET and a leadframe structure with a source lead and a gate lead would not decrease the amount of circuit board real estate that is occupied by Tsuda et al.'s package, or decrease its complexity or cost. For example, the amount of real estate occupied by Tsuda et al.'s package, as modified with a power MOSFET and a leadframe structure with a source lead and a gate lead, would be the same in both cases. Accordingly, contrary to the obviousness rejection, modifying Tsuda et al.'s package with Kasem et al.'s "process" would not result in an improved package, let alone package that is "simpler" or "less expensive" as alleged by the Examiner.

2. *Obviousness has not been established, since modifying Tsuda et al.'s surface acoustic wave device with a vertical power MOSFET, and a leadframe structure with a source lead and a gate lead would be contrary to the intended purpose of Tsuda et al.*

Obviousness has not been established, since modifying Tsuda et al.'s surface acoustic wave device with a vertical power MOSFET, and a leadframe structure with a source lead and a gate lead would be contrary to the intended purpose of Tsuda et al. As stated by the Court of Appeals for the Federal Circuit and the MPEP:

> If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). MPEP 2143.01.

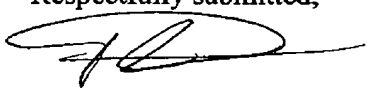
Here, paragraph [0026] of Tsuda et al. states that "[a]n object of the present invention is to provide the low-provided surface acoustic wave device that increase the attenuation volume in the high-frequency attenuation band..." Here, if one were to modify Tsuda et al. to substitute Tsuda et al.'s surface acoustic wave device with Kasem et al.'s power MOSFET (and corresponding leadframe structure), one would no longer be producing an "surface acoustic wave device," and the "object" of Tsuda et al.'s invention would no longer be satisfied. Since the modification proposed by the Examiner would make Tsuda et al.'s device unsatisfactory for the intended purpose of Tsuda et al.'s device, there is no motivation to modify Tsuda et al. to arrive at the claims and obviousness has not been established.

CONCLUSION

In view of the foregoing, Applicant believes all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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